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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 20

Application Number: 09/812,733
Filing Date: March 19, 2001
Appellant(s): TREMBLAY ET AL.

David W. O'Brien
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 20, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The active claims are 29-38. Appellants propose to cancel claims 30-32 and 36. Claims on appeal are therefore 29, 33-35 and 37-38.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is incorrect.

The two Rule 116 amendments (paper # 10 and 17) have not been entered. The amendments proposed to change scope of claims 33 and 34 and to cancel claims 30-32 and 36 after final rejection, which require further consideration. In the final disposition of the instant application, the paper number 17 amendment will be entered in part to cancel claims 30-32 and 36.

(5) Summary of Invention

Two embodiments of a context switching controller are respectively shown in Figures 5 and 6. The difference between Figures 5 and 6 is that Figure 6 shows in

addition a dirty bit enable storage 620. Since the dirty bit enable storage is not recited in any of the appealed claims, Figure 6 is not relevant to the instant Appeal.

Figure 5 shows 1. an instruction register 515, 2. a register file 510, 3. a dirty bit logic 514 and 4. a dirty bit storage 512. Instruction register 515 and register file 510 are basic components of a processor. Appellants' invention is a context switching controller which consists of the remaining two components, namely, dirty bit logic 514 and dirty bit storage 512 as shown in Figure 5. Register file 510 has 256 registers. Instruction register 515 has five fields. The last field is an address for addressing register file 510. Only the three most significant bits of the address are sent to Dirty bit logic 514. The three bits (2^3=8) give the dirty bit logic 514 the capability to address eight locations. Therefore, as far as the dirty bit logic 514 is concern, register file 510 is divided into eight groups with 32 registers in each group. The dirty bit logic 514 addresses the register file 510 in groups and not in individual registers. Each of the eight groups is associated with a functional unit, for example, an integer arithmetic logic unit or a floating point arithmetic logic unit, etc. See Appellants' Figure 4. The functional units use their associated register file (register groups) to perform arithmetic operations, to store operands, intermittent results and final results of the arithmetic operations.

OPERATION OF THE CONTEXT SWITCHING CONTROLLER

When dirty bit logic 514 receives the three bits address from instruction register 515, it determines whether the processor reads or writes from the register file 510. If it is a write-access, dirty bit logic 514 sets the corresponding dirty bit in the dirty bit storage 512 for indicating that the accessed register group has data stored in it.

HOW THE CONTEXT SWITCHING CONTROLLER IS BEING USED

A context switching controller is an interrupt controller. Consider the following scenario: a processor receives a request to process job B which has higher priority while it is currently processing job A. In order for the processor to continue job A from where it left off after it has taken care of the request, the processor must transfers the job A data stored in the register file to other places before it switches to process job B. The processor then is able to use the register file to process job B. After it is done with job B, the processor will transfer the job A data back to the register file. The processor then is able to continue where it left off before the job switching. Applicants' invention is to use dirty bit logic 514 and the dirty bit storage 512 to identify those storage groups in the file register which have data stored in it. When job switching comes, only those identified groups are required to have their data saved at other places.

(6) Issues

The active claims in the instant application are 29-38. The double patenting rejection of claims 29, 34-35 and 37-38 is withdrawn in view of the Terminal Disclaimer. Claims 29, 33 and 35 are allowed in view of the Terminal Disclaimer. The remaining issue is whether the rejection of claims 34, 37-38 under 35 USC 103(a) is proper.

(7) Grouping of Claims

Group I: Claim 34, 37 and 38 stand rejected under 35 USC 103(a) over Emer. Claims 37 and 38 stand or fall with claim 34.

Group II. Claims 29, 33 and 35 allowed.

Group III. Claims 30-32 and 36, withdrawn from consideration because Appellants propose to cancel the claims.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,470,443	Emer et al.	10/2002

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 34 and 37-38 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Emer (USP 6,470,433).

The Board's attention is respectfully directed to Instruction Register 30, Functional Units 34 (such as I/O units and Arithmetic Logic unit, lines 44-45 of column 4) and Register file 32 in Figure 2 of Emer, and the description in lines 3-10 of column 5. Emer teaches a controller in a processor comprising:

a data storage unit (Registers 32) divided into a plurality of storage groups (the processor of Emer has more than one functional units and the registers are divided among the plurality of functional units);

a dirty bit storage (the collective valid bits, line 4-5 of column 5) coupled to the data storage and including one or more storage bits (valid bits of Emer) corresponding to one or more respective storage groups in the data storage unit; and

a dirty bit logic (the circuit in Emer which sets the valid bits, lines 4-5 of column 5) coupled to the dirty bit storage and configured to receive a destination address of one or more instructions executing on the processor.

As can be seen, Emer meets all the structural limitations recited in the body of the claims. The sole difference is that the vlaid bit apparatus of Emer is not in a context switch controller. However, it is noted that the components as recited in the claim have nothing related to context switching (interrupt). The claim did not recite that the dirty bits are for identifying registers having data to be saved in the event of interrupt. Nor the claims recite that only those registers identified by the dirty bits are saved in the event of interrupt. The dirty bit storage and logic as recited in the claim are merely for separating the registers into those which have their dirty bits set and those not set. Emer teaches a valid bit apparatus for identifying those registers in a register file which are written (having valid bits set) and those which have not been written (valid bits not set). From the teaching of Emer, it would have been obvious to a person of ordinary skill in the art to use the valid bit storage and set logic for classifying registers in accordance with certain conditions (written or not written) in a context switch controller if the register file in a context switch controller is required to be classified or differentiate from each other.

(11) Response to Argument

With respect to the remarks directed to the 103 Rejection,

Appellants did not disagree that Emer meets all the structural limitations recited in the claim body. Appellants' argument for patentability is solely based on "context switch controller" recited in the preamble. Appellants contend that the valid bit storage and set logic of Emer are not related to context switching. So does claim 34. The dirty bit storage and logic as recited in claim 34 have nothing to do with context switching either. The preamble in the present form did not even set forth intended use. The claim did not recite functional relationship between the components nor how they interact in context switching. The preamble, when read in the context of the entire claim, merely set forth at best that the dirty bits and logic are being comprised in a context switch. No patenting weight is given to the preamble (MPEP 2111.02).

For the above reasons, it is believed that the propriety of the rejections remains intact. It is therefore respectfully requested that the rejections be sustained.

Respectfully submitted,

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April 15, 2004

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